Prototyping and Implementing Flight Qualifiable Semicustom CMOS *P*-Well Bulk Integrated Circuits in the JPL Environment

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Presently, there are many difficulties associated with implementing application specific custom or semi-custom (standard cell based) integrated circuits (ICs) into JPL flight projects. One of the primary difficulties is developing prototype semi-custom integrated circuits for use and evaluation in engineering prototype flight hardware. The prototype semi-custom ICs must be extremely cost-effective and yet still representative of flight qualifiable versions of the design. A second difficulty is encountered in the transport of the design from engineering prototype quality to flight quality. Normally, flight quality integrated circuits have stringent quality standards, must be radiation resistant and should consume minimal power. It is often not necessary or cost effective, however, to impose such stringent quality standards on engineering models developed for systems analysis in controlled lab environments. This article presents work originally initiated for ground based applications that also addresses these two problems. Furthermore, this article suggests a method that has been shown successful in prototyping flight quality semi-custom ICs through the Metal Oxide Semiconductor Implementation Service (MOSIS®) program run by the University of Southern California's Information Sciences Institute. The method presented has been used successfully to design and fabricate through the MOSIS three different semi-custom prototype CMOS p-well chips. The three designs make use of the work presented here and were designed consistent with design techniques and structures that are flight qualifiable, allowing one hour transfer of the design from engineering model status to flight qualifiable foundry-ready status through methods outlined in this article. The design techniques presented here that permit the flight qualifiable prototyping arose as a natural extension of other purely ground-based work that will also be described.

I. Introduction

Recently, during the course of developing a standard cell library for use in ground based applications for the Deep Space Network (DSN), a new method and set of standard cells was also developed, almost with no additional work, that addressed many of the flight quality prototyping issues that are critical to the use of custom integrated circuits in JPL flight projects. The general process of bringing a new standard cell family online for use in ground application microcircuit design at JPL is not unlike that process necessary to develop the capability to prototype flight quality custom ICs for flight projects. As one looks to the future of space investigation, it is clear that the widespread, successful use of

custom integrated circuits (ICs) in NASA flight projects and ground signal processors will hinge on the ability of NASA personnel to maintain full design cognizance of those circuits.

Although custom ICs have already been used in major flight projects at JPL, they have been used only on a very limited basis. Such limited use allows the electrical and physical environment to be precisely defined so that it is possible to make effective use of non-JPL personnel for custom IC design. The future economics of unmanned space exploration, however, point toward the use of multi-mission hardware and equipment.[1] The need to design multi-mission hardware in turn points toward an increasing use of custom and semi-custom integrated circuits, whose replication cost in time, money *and* mission risk is extremely low (Ref. 1). If whole flight subsystems are then designed around several custom integrated circuits, it will not be possible technically nor economically to maintain control and cognizance over flight hardware without involving JPL custom microcircuit designers directly.

Let us diverge for the next few paragraphs and investigate what might be needed to enhance JPL's ability to use custom microcircuits in flight projects. This short investigation will help us understand the parallels of ground based and flight quality prototyping IC development. In order to allow JPL personnel to effectively use custom and semi-custom ICs in flight quality hardware, three things are necessary:

(1) Engineering prototype chips must be available quickly, reliably and for extremely low cost in small quantities, and must reflect the flight quality chip speed performance, architecture, and testability.

(2) Transfer of the design from engineering prototype to flight quality foundry ready must be done without redesign or exposure of the design to operations that may affect chip size, pin-out, power consumption, floor plan or architecture. Nevertheless, the flight quality design must fully address all issues of reliability and radiation resistance.

(3) The flight quality design must be consistent with designs and foundries that have a proven success record and have demonstrated qualified custom ICs in the past.

Given that set of ground rules, if one were interested in real prototyping capability, it would then be necessary to choose a particular integrated circuit technology to further focus the development of a method for prototyping flight quality custom ICs. For technical reasons that are well outlined in the literature (Ref. 2), and for its availability and history of use in qualified systems, one would probably choose bulk CMOS *p*-well for the design of custom integrated circuits in the near future. Bulk CMOS *p*-well offers extremely low power operation with wide noise margins and immunity to power supply fluctuation. Even more important for the economically strained flight project reality, bulk CMOS *p*-well is much cheaper to produce than other technologies that have the same or lower reliability and radiation resistance.

To further focus a hypothetical effort on developing technology to permit rapid and effective use of custom ICs in JPL flight projects, one would also consider the JPL design environment. In order to be effective, prototype flight quality custom ICs would have to be designed quickly, by designers with a firm knowledge of the target system's functional and timing constraints and some simple rules of reliable, testable and radiation resistant architectures. Those designers could be expected to have little detailed IC design expertise or detailed knowledge of silicon structures and device physics. That typical designer profile would point the way to implementing custom integrated circuits with standard cells rather than fully hand crafted structures. Standard cells provide nearly the density of hand crafting and yet free the designer from detailed and esoteric analysis that is necessary to properly build digital logic gate structures in silicon for space flight and prototype custom ICs. Further gains on the density of hand crafting could be had by hand placing standard cells in designs that must be dense, as opposed to allowing placement of cells by automatic computer tools.

Up to now, we have investigated in general terms what might happen if there were an effort to develop a comprehensive capability to design and implement custom microcircuits in JPL flight projects. We can, however, continue the conjecture in more detail. The directives outlined above indicate the following possible approach to achieving the ability to quickly and accurately obtain engineering prototype custom ICs for flight quality prototype hardware:

(1) Search for a CMOS *p*-well bulk standard cell family that has an outstanding flight quality performance history when fabricated through the supporting foundry.

(2) If such a standard cell family is found, determine what modifications would be necessary to fabricate the cells through the inexpensive, readily available MOSIS foundry service, with the understanding that the MOSIS design rules must be met in order to get typical MOSIS yield and performance. It is assumed that the MOSIS performance levels are adequate for

[1]Jordan, J. J., Getaway Special Project Manager, Physical Science Laboratory, Private Communication, June 1984.

engineering prototypes. Also determine if interconnection structures designed to the MOSIS design rules would meet the design rules of the original foundry. If so, then proceed.

(3) If the individual standard cells from the selected family can be modified under the constraints outlined below then do so; verify (Ref. 3) the results by fabricating through the MOSIS.

   (a) Modified cells shall be of the same bounding size, port placement and power bussing as the original cells. The periphery and connectivity of the modified cells will be identical to the original cells.

   (b) Modified cells shall have the same transistor structures and drive capability (size) as the original cells in order to maintain similar performance between original and modified cells.

   (c) Modified cells must not contain any structures that would result in MOSIS or original foundry design rule violations with any possible adjacent structures.

   (d) No modifications to the original cells can be made.

(4) If the verification-through-MOSIS results from Step 3 are positive, then develop a method for designing with modified cells and then substituting original cells without exposure of the design to normal modification and design operations that could introduce human error.

(5) Verify with computer aided analysis that designs done to MOSIS design rules, with original cells subsequently substituted for modified cells, do in fact meet the design rules of the original foundry.

(6) Verify the design sequence by fabricating the same design through the MOSIS *and* the original foundry, using appropriate cells for each, and compare performance.

(7) If performance comparisons are favorable then release, with appropriate legal agreements, two sets of standard cells of identical function and port placement and of similar performance. One set of modified cells is suitable for fabrication through the MOSIS, and the original untouched library of cells can be fabricated through the originating, high reliability, flight qualifiable foundry. Also release the means for substituting original cells for modified cells without affecting the design floor plan or architecture.

We have now investigated to a detailed planning level what would be involved in developing prototyping capability for flight project custom microcircuits at JPL. Although the above approach may seem special, perhaps peculiar only to the specific interests of flight projects, the approach outlined above has only minor differences with the work that is necessary to bring any typical vendor's standard cell family to JPL for use in ground applications. In fact, in the course of bringing on-line a standard cell family for ground based applications, all items in the list above have been completed up to, but not including, Step 6.

A standard cell family was found that looked suitable for use in DSN applications and it was decided to proceed with the necessary modifications to make the cell library more widely useful at JPL, thus spreading future maintenance costs over more users. It typically takes 2 to 3 years to design and verify an entire cell library from scratch, so it was determined that a suitable alternative would be to modify an existing cell library for use within the existing JPL design framework. Those modifications typically amount to changes to the mask layer names, changes to mask geometry to meet the MOSIS design rules and then subsequent verification through the MOSIS.

The standard cell family chosen to bring to JPL was Sandia National Laboratories' $4/3\mu$ CMOS p-well Bulk radiation hardened cell library (Ref. 4). The library was chosen for its completeness, its ease of use, easily available documentation and the fact that minimal modifications were needed in order to use the cell library with the MOSIS for ground based applications. Furthermore, since Sandia is also a government agency, there were no legal difficulties or licensing fees needed to get the cell library information from Sandia. Sandia's excellent reputation and historical record of producing flight quality and mil-spec semi-custom ICs for military and spaceflight applications was also intriguing, but not of primary concern at the time. Of course, it was realized that those structures in the Sandia cells that were necessary for flight quality results would not and could not be fabricated through MOSIS. That fact was irrelevant, though, because the new modified cell library was targeted only for ground applications.

As work began in modifying and bringing the Sandia cell library on-line for JPL ground based use and MOSIS fabrication, little consideration was given to maintaining any compatibility with the original Sandia cells. It soon became apparent, though, that if slightly stricter modification guidelines were used, namely, those numbered 3 through 7 in the approach outlined above, not only would a useful cell library for ground based work be obtained, as was originally desired, but also, a set of standard cells that permitted quick prototyping of flight quality custom ICs could be had. It was clear that the items 1 and 2 in the approach outlined above

had already been met simply by our choice of the original Sandia cell family.

The more stringent guidelines were, in fact, adhered to, and the same cell library can now be used for ground based and flight prototyping applications. The rest of this article will outline a summary of the problems, methods and analysis of reconstructing Sandia cells to MOSIS standards guided by the constraints outlined above, concentrating on the more interesting flight prototyping characteristics that came out of this work. The article will also address the problems and methods of implementing modified Sandia cells, hereafter referred to as MOSIS cells,[2] in designs. Results and limited analysis of MOSIS fabrication verification will also be presented.

II. Design Rule Comparison

Table 1 lists important differences between the MOSIS design rules for 3μ bulk CMOS p-well (Ref. 5) and Sandia's $4/3\mu$ bulk CMOS p-well radiation hardened process (Ref. 6). The most important differences that affect the modification of the cells are first level metal minimum width and contact overlap requirements. Although the MOSIS requires much more contact overlap than Sandia, some help in cell internal modification space availability is lent by the 1μ smaller minimum metal width for the MOSIS. One can see by the poly and metal contact and poly and metal spacing and width rules that interconnection structures satisfying the MOSIS design rules will also satisfy Sandia's design rules. That fact is of critical importance for avoiding two design iterations in the advancement from prototype to flight quality.

Table 2 lists the layers that are used by the MOSIS (Ref. 5) and Sandia (Ref. 6) in their respective CMOS p-well processes. This table shows radical differences between the specification of diffusion masks. The diffusion mask specification differences have a profound effect on many of the modifications and performance of the MOSIS cell based designs and will be discussed later. Two additional layers that are present in the Sandia line that are not available through the MOSIS are the P+ guard ring and the V+ threshold adjust implant. The guard ring and the threshold adjust are included in Sandia's line to combat latch-up and body-effect threshold degradation in radiation environments and thus are unnecessary in the prototype MOSIS cells.

The only layers available through the MOSIS that are not available through Sandia are the second level metal and contact cut to first level metal. The use of second metal interconnections in MOSIS designs can offer a speed improvement of up to a factor of 3 over designs using polysilicon for interconnections. Such a speed improvement is not representative of Sandia fabrication since second level metal is not available on Sandia's $4/3\mu$ line. Therefore, interconnections using second metal are not permitted in prototype designs. If second metal were used in prototype designs, transfer of the design to Sandia for fabrication would require redesign of the interconnections, which violates one of the ground rules of the prototyping endeavor. Second metal must be used, however, in the modified Sandia bonding pad cells at the bonding pads. If second metal is not present at the bonding pads, the MOSIS bonding operation will attempt to wire bond to the insulating material between metal one and metal two and an unsatisfactory connection will result.

III. Modification Synopsis

Figure 1 shows an unmodified Sandia cell with Sandia layers. Table 3 shows the correspondence between the layer names and the plot names. The n channel field effect transistors (nFETs) are contained in the guard ring at the bottom and the p channel FETs are along the top. The power bus is also at the top and ground is at the bottom. The polysilicon gates are 3μ long and the gate width direction runs vertically. Figure 2 shows the same cell modified for fabrication through the MOSIS. Layers have been deleted and modified as necessary to meet the MOSIS design rules both internally and to possible adjacent structures. The modified cell still maintains the original functionality, periphery physical characteristics and approximate transistor sizes as the cell shown in Fig. 1.

Since Sandia makes use of a deep P+ guard ring surrounding the p-well, it is permitted in the Sandia cell to cross the p-well boundary with thin oxide. The width of the Sandia cell nFETs is then controlled by the height of the n+ implant mask. (Note that Sandia actually implants source and drain regions in order to avoid the high temperature processing required for diffusion. High temperature processing undermines the radiation resistant characteristics built in prior processing steps.) Since the MOSIS supports neither a guard ring nor an explicit definition of the n+ diffusion mask, the MOSIS version of the cell must be modified to reflect that fact.

First, the thin oxide edge must be brought inside the p-well boundary in the nFET locale. Since all thin oxide in MOSIS designs is either diffused p+ or n+, a shorting forward biased condition between the grounded p-well and the biased substrate outside the p-well would exist if the thin oxide were permitted to cross the p-well and subsequently allow n+ diffusion under its area.

[2]Not to be confused with the MOSIS Charger cell library released by MOSIS. In the context of this article, the term "MOSIS cells" refers to Sandia cells modified for fabrication through MOSIS.

Second, the width of the nFETs must be controlled by the thin oxide mask rather than by the unavailable $n+$ diffusion mask. Figure 3 shows the modifications in the nFET locale from the Sandia cell on the left to the modified MOSIS compatible cell on the right.

One may also note by comparing Figs. 1 and 2 that the MOSIS cell has substantially more contact overlap of the contacting layers than the original Sandia cell. This is necessary to meet the MOSIS design rules. Although intuition might lead one to believe that the oversized looking metal lines in the MOSIS cell would increase node capacitance significantly, the typical increase in capacitance due to increased metal area around the contacts is not substantial enough to be of interest. SPICE (Ref. 7) simulations of the MOSIS and Sandia cells show that the electrical circuit is essentially unaffected by the slight differences in node capacitance between the Sandia cell and its MOSIS counterpart.

Cells were modified using Caesar for geometrical manipulation and Lyra for design rule checking to MOSIS specifications (Ref. 8). It was necessary in special situations to push some conservative minimums by $1/2\mu$ in order that the modified cell maintain the same bounding dimensions as the original Sandia cell. The two design rules that were violated approximately 3% of the time were the first metal to first metal spacing (was made 3.5μ instead of 4μ) and the contact to channel spacing (was made 2.5μ instead of 3μ). Since the MOSIS design rules are a conservative superset of design rules for many foundries, it was estimated that pushing the design rule limits in such a manner would have minimal effect on yield. To date, none of the 72 chips returned from the MOSIS have shown any indication of poor performance or failure due to these design rule violations.

IV. Method of Transferring From Prototype to Flight Quality

Given that now two sets of outwardly identical cells exist, it is relatively simple to transfer a design consisting of interconnections and MOSIS cells to one consisting of the same interconnections and Sandia cells. The transfer assumes that the MOSIS prototype design has accounted for architecture and timing requirements appropriate to flight quality designs.[3] Again, a constraint is placed on the interconnections to not employ second level metal.

The use of the Caltech Intermediate Format (CIF) as the design database provides a quick means through symbol calls to effect the desired cell switch (Ref. 9). The entire design is completed with MOSIS cells and then transferred with the cell calls only (not the cell symbol definitions) to another environment where the cell symbols are defined as Sandia cells. Care is taken by the design tool maintainer to insure that CIF layer names are consistent throughout Sandia and MOSIS representations. A typical design sequence might proceed as follows on a UNIX® system using the Berkeley Computer Aided Design tool set:

(1) The designer constructs the design with his choice of tools and the MOSIS cells. The designer is only constrained at this point to produce a physical representation of the design in CIF that is constructed using MOSIS cells and design rules. Such construction might be accomplished by using Caesar or Magic (Ref. 10) to construct the design in a UNIX directory that only contained MOSIS cells with Caesar's or Magic's path then set to that working directory.

(2) The design is design rule checked and sent in CIF format to the MOSIS for fabrication (Ref. 11).

(3) The design is transferred into a new UNIX directory that contains all of the information that existed in the original directory except for the representations of the MOSIS cells. This is done with a UNIX copy command. The Caesar or Magic path is set to the new directory and the original Sandia cells are copied from a master directory into the new directory. It is critical that the MOSIS cells have the identical call names as their Sandia counterparts.

(4) The design is write change protected and brought up for read only editing by Caesar or Magic in the new directory. The tools automatically invoke the Sandia cells where the MOSIS cells were previously. The design is written out with a new name and is immediately write protected.

(5) The design is design rule checked and sent to Sandia or a suitable second source in CIF format, or in the more industry accepted GDSII format, for mask making and fabrication.

V. MOSIS Verification and Performance Results

To date, three different designs have been fabricated through the MOSIS. The first consisted of large sections of shift registers and test cells. The fabricated chips were tested and found functional but with higher operating current and slower speed than expected, based on simulations. A problem in substrate biasing and p-well isolation within the cells was inferred and modifications were made to adjust diffusion

[3] A survey and analysis of specific architecture and timing characteristics desirable for achieving flight qualification is beyond the scope of this article.

masks to provide better connectivity and correct the biasing problems.

Those modifications proved helpful to the second design, which was actually very similar to the first. The second design exhibited normal speed and only slightly increased power consumption over normal. Further modifications to diffusion masks were made and a third design, much different than the first two, was completed with the modified cells and sent to the MOSIS for fabrication.

The third MOSIS design exhibited much higher speeds than worst case simulations. This was partly due to careful hand calculations of buffering and loading in the circuit architecture and partly due to the success of the modifications from the first two designs. A third factor relating to the polysilicon may have also been a factor and is discussed below. The third design was fully static and functioned at clock rates from DC to 22 MHz. Microprobing of individual gates indicated loaded gate delays on the order of 3 to 5 nanoseconds. Unfortunately, there was still a problem with excessive power dissipation.

The higher than expected speed exhibited by the third design, which was an array of quasi-synchronous counters, may be attributed in part to the $n+$ diffused polysilicon used for interconnections in the MOSIS fabrication. Such polysilicon would not be expected in a typical Sandia fabrication. Since the designer only specifies the $p+$ diffusion mask to the MOSIS and the MOSIS generates the $n+$ diffusion mask as the complement of the $p+$ mask, most of the polysilicon interconnections in the MOSIS design are exposed to the $n+$ diffusion operation. Since diffused polysilicon has a much lower resistivity than implanted or *in situ* doped polysilicon (Ref. 12), circuit interconnection RC time constants are somewhat smaller in designs with diffused polysilicon interconnections. Sandia generates $n+$ and $p+$ regions with implanting techniques rather than diffusion techniques and furthermore does not allow implanting of most of the polysilicon used for interconnections. More investigation of the exact differences between the resistivities of Sandia's typical polysilicon and the MOSIS typical polysilicon is needed.

Unfortunately, differences in polysilicon interconnection resistivity cannot come close to accounting for the high speeds. Other factors also contributing to high operational speed of the third design include maximum use of metal for interconnections, carefully analyzed buffering of critical signals (mentioned above), careful hand placement of cells and manual floor planning that minimized interconnection length. The P-well doping concentrations may also be a major factor in the high observed speed.

The increased power consumption in the third MOSIS design may be at least in part attributed to the inability of the designer to explicitly specify the $n+$ diffusion mask to the MOSIS. Since the designer cannot explicitly specify the $n+$ diffusion mask, the designer has very little control over the pad protection diode junction characteristics. Initial investigation[4] indicates that high reverse currents may be present between supply rails in pad protection diodes (see Figure 4). The Sandia cell protection diodes, in fact CMOS diode structures in general, do not lend themselves well to obtaining good performance without the ability to specify both the $n+$ and $p+$ diffusion masks explicitly. Further testing is necessary to verify that the excess currents are, in fact, flowing through the pad protection diodes.

The third MOSIS design also contained many individual cells with probe pads for individual testing. Three different sizes of inverter logic and buffer cells were tested for electrically induced latch-up susceptibility, with favorable results. The inverters were powered at 3 volts and driven to a -2 and +5 volt logic signal input without latching up. Next the inverters were powered at 5 volts and subject to a -5 to +10 volt logic signal at 1 MHz. Again there was no latch-up. Finally the inverters were powered at 6 volts and driven with a -5 to +10 volt logic signal at 1 MHz that had an additional 3 volt transient spike induced on both the rising and falling edges. The inverters still did not latch up. There was no purposeful on-chip signal clamping or special probe pad structures used in conjunction with these tests. The tests indicated excellent localized latch-up resistance for the MOSIS cells. A test was not devised to observe chip-wide latch-up susceptibility.

In summary, designs fabricated through the MOSIS with the modified Sandia cells have exhibited very good performance and robustness. Although the MOSIS designs have not been tested at 10 volts (a typical operating voltage for a Sandia chip) because they were fabricated by a 5 volt line. There are no expected problems concerning supply voltage in transferring from MOSIS to Sandia.

One possibly serious problem that may arise, though, is in attempting to operate with high supply voltages in the other direction. That is, attempting to operate MOSIS prototype designs at the same supply voltage that Sandia designs will operate at comfortably. The MOSIS bases most of its fabrication parameters on up to 6 volt operating supply, while Sandia typically fabricates for up to 10 volts and beyond. The problem would appear when operating a prototype MOSIS design in hardware running at typical flight system supply voltages of 10 volts and greater. For flight systems employing 5 volt supply voltages, no prototyping problems are expected.

[4]Shafer, B. D., Sandia National Laboratories. Private Communication, May 1986.

VI. Conclusions and Future Work

A method and set of standard cells has been developed that permits not only quick ground application microcircuit development, but also easy and extremely high confidence prototyping of flight quality standard cell based custom microcircuits. The flight prototyping method has been tested up to actual fabrication by the flight quality foundry. Despite any differences in the electrical performance of the prototype designs compared to typical flight quality performance, a high degree of confidence in the design can be obtained for very low cost before the decision is made to include a custom microcircuit in a flight system. Also, it is possible to evaluate architecture and timing constraints with real hardware in the lab by prototyping potential flight quality custom microcircuits through MOSIS. The job of prototyping and obtaining flight qualifiable chips has been reduced to a single design iteration with a simple "human-free" substitution method for going from prototype to flight quality foundry-ready.

But not to be overshadowed by flight applications, a reasonable general purpose standard cell library for routine use with the MOSIS has also been generated. Routine use of this new cell library has the advantage of possibly permitting a quick development of flight quality chips for designs that may not necessarily have been originally intended to fly.

Future work will include more definitive analysis and characterization of electrical parametric operating differences between MOSIS and Sandia fabrications. Work is presently proceeding, under other funding, on an actual flight project prototype design for Mariner Mark II. The prototype chip is a digital filter containing adders, multipliers and other functions and is built entirely from modified Sandia cells. The prototype is in fabrication with the MOSIS at the time of this printing. It is hoped that the circumstances will present an opportunity to fabricate the prototype through a flight quality foundry after substitution of the flight quality cells. Such an opportunity could further verify the work and methods introduced here.

Future work will also include analysis of Sandia's new 2μ CMOS p-well, double metal cell library. Initial surveys[5] indicate that the new radiation hardened 2μ library will be capable of direct fabrication through MOSIS without modification. Another good ground based cell library would be had and radiation hardened performance would then become purely a product of the fabrication line rather than both the cell structure and the line.

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[5]Bair, R. E., Barnard, W. J., Shafer, B. D. (of Sandia National Laboratories), Olson, E. M. (of JPL) and Steelman, J. E. (of New Mexico State University), Technical Discussions at Sandia National Laboratories, Albuquerque, New Mexico, 1985.

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Table 1. Important design rules for cell modifications

Design Rule	Sandia Rule, μ	MOSIS Rule, μ
Min. metal line	4	3
Min. metal space	4	4
Min. poly line	3	3
Min. poly space	4	4
Min contact to gate	2.5	3
Metal overlap of contact	0.5	2

Table 2. Layer sets for Sandia and MOSIS

Layer	Sandia	MOSIS
Polysilicon	Yes	Yes
Thin Oxide	Yes	Yes
Threshold Adjust	Yes	No Access
Metal One	Yes	Yes
Metal Two	No	Yes
Contact	Yes	Yes
Via (m1-m2)	No	Yes
P-Well	Yes	Yes
P+	Yes, implanted	Yes, diffused
N+	Yes, implanted	No, diffused, logical not of P+
P+ Guard Ring	Yes	No

Table 3. List of layer names and plotted names for Figs. 1, 2 and 3

Layer Name	Plot Name
Polysilicon	CP
Thin Oxide	CA
Threshold Adjust	CX
Metal One	CM
P-Well	CW
P+	CS
Contact	CC
N+	CT
P+ Guard Ring	CG

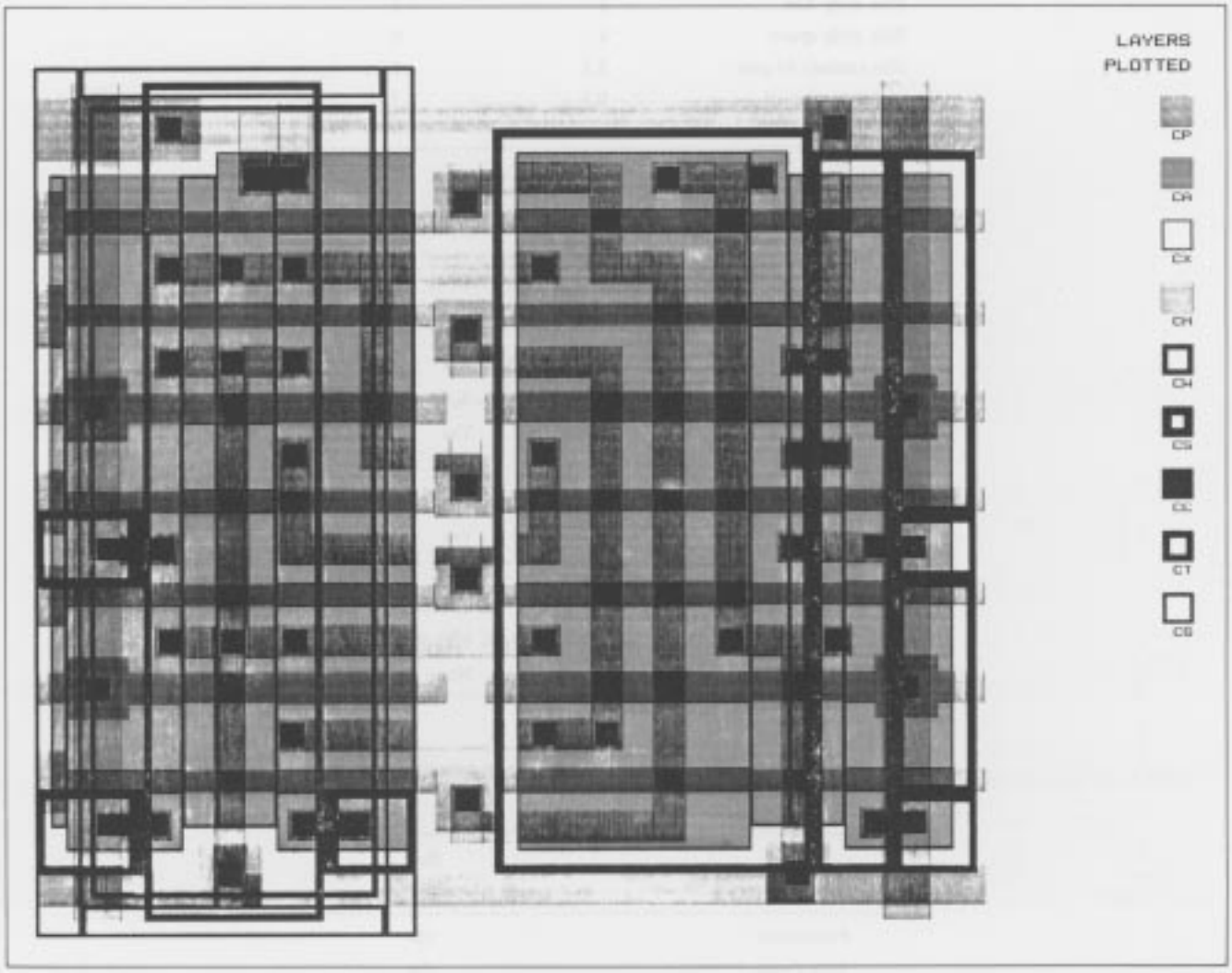

Fig. 1. An original Sandia cell showing the guard ring and overlap of *p*-well edge by thin-oxide

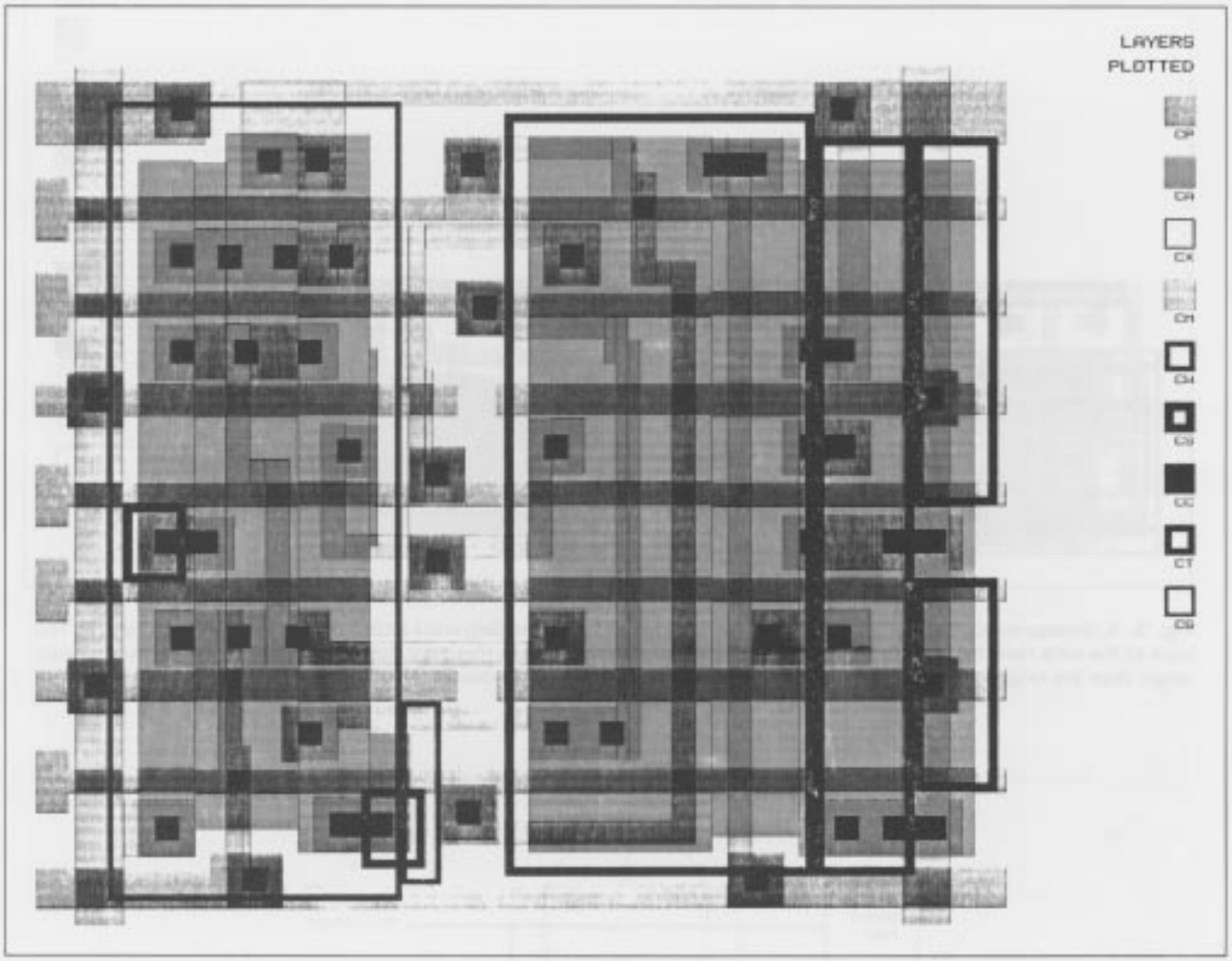

Fig. 2. A modified Sandia cell suitable for fabrication through the MOSIS

Fig. 3. A closeup comparison of the nFET regions of an original Sandia cell (left) and a MOSIS or modified Sandia cell (right). The tops of the cells have been chopped off for illustrative purposes only. Note that the modified cell's nFET gate width is slightly larger than the original cell's in order to accommodate some necessary contacts.

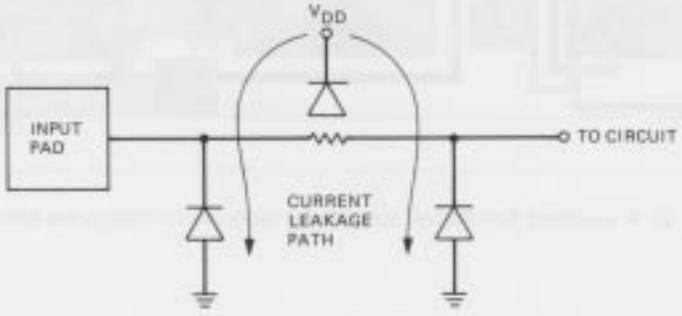

Fig. 4. Schematic of input pad circuitry showing possible path of high power supply currents due to input protection diode leakage